PRODUCT SPECIFICATION

12.1” TFT LCD MODULE
MODEL: YDP LCD I 1210 LVDS

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
-	TFT S. G. H 20240531	TFT 周福云 20240531	TFT L. L 20240531

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2024.05.31	LL	Initial Release	

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	12.1”	
LCD type	IPS TFT	
Display Mode	Transmissive / Normally Black	
Resolution	1024 x 768	Pixels
View Direction	FULL VIEW	Best Image
Module Outline	260.5(H) x 204(V) x 7.3(T) (Note1)	mm
Active Area	245.76 (H) x 184.32(V)	mm
Pixel Pitch	240(H) x 240(V)	um
Pixel Arrangement	RGB Vertical stripe	
Polarizer Surface Treatment	Anti-Glare	
Display Colors	16.7 M	
Interface	LVDS	
Driver IC	JD9168S	-
With or Without Touch Panel	Without	
Operating Temperature	**-0～50**	ºC
Storage Temperature	**-10～60**	ºC
Weight	TBD	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25ºC

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	-0.3	6.3	V
	IOVCC	-0.3	3.6	V
Storage temperature	T_{stg}	-0	+50	ºC
Operating temperature	T_{op}	-10	+60	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.5	3.3	6.0	V
	IOVCC	2.5	-	3.3	V
Logic Low input voltage	V_{IL}	0	-	0.3*IOVCC	V
Logic High input voltage	V_{IH}	0.7*IOVCC	-	IOVCC	V
Logic Low output voltage	V_{OL}	0	-	0.2*IOVCC	V
Logic High output voltage	V_{OH}	0.8*IOVCC	-	IOVCC	V
Differential input high threshold voltage	Rx_{VTH}	+0.1	+0.2	+0.3	V
Differential input low threshold voltage	Rx_{VTL}	-0.3	-0.2	-0.1	V
Input voltage range (singled-end)	Rx_{VIN}	0.7	-	1.7	V
Differential input common mode voltage	Rx_{VCM}	1.0	1.2	1.4	V
Current Consumption All White	I_{DD+} I_{IO}	-	TBD	-	mA

5. Backlight Characteristic

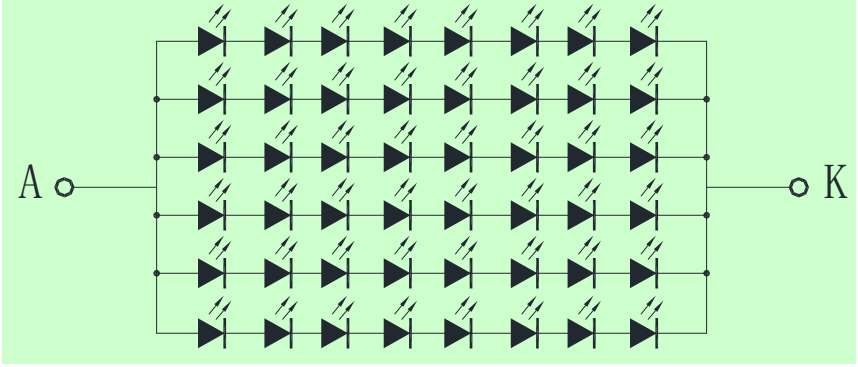
5.1. Backlight Characteristic

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta=25 ºC, I_F=60mA/LED	22.8	**24.8**	27.2	V
Forward Current	I_F	Ta=25 ºC, V_F=3.1V/LED	-	**360**	-	mA
Power dissipation	P_D	-	-	**8928**	-	W
Uniformity	Avg	-	-	80	-	%
LED working life(25℃)	-		-	30000	-	Hrs
Drive method	**Constant current**					
LED Configuration	42 White LEDs (8 LEDs in one string and 6 groups in parallel)					

Note1：LED life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at Ta=25±2 ºC,60%RH±5%, I_F=60mA/LED.

5.2. Backlighting circuit



6. Optical Characteristics

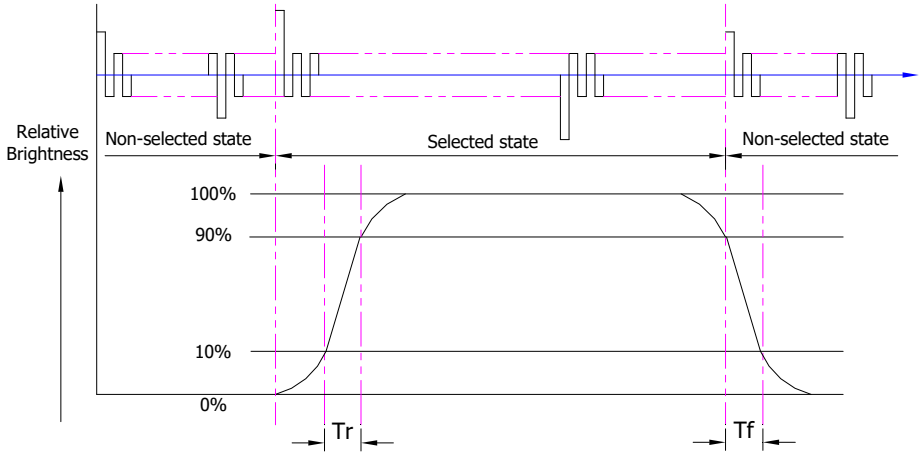
6.1. Optical Characteristics

Ta=25ºC,VCI=3.3V

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Luminance on TFT(I_f =60mA/LED)		Lv		280	350	-	cd/m²
	Contrast ratio(See 6.3)		CR		1000	1200	-	
	Response time (See 6.2)		TR		-	25	30	ms
			TF					
	Chromaticity Transmissive (See 6.5)	Red	XR	Backlight is on	-	TBD	-	
			YR		-	TBD	-	
		Green	XG		-	TBD	-	
			YG		-	TBD	-	
		Blue	XB		-	TBD	-	
			YB		-	TBD	-	
		White	XW		-	TBD	-	
			YW		-	TBD	-	
	Viewing Angle (See 6.4)	Horizontal	θX+	Center CR≥10	75	85	-	Deg.
			θX-		75	85	-	
		Vertical	φY+		75	85	-	
			φY-		75	85	-	
	NTSC Ratio(Gamut)		-	θ=0º	65	70	-	%

6.2. Definition of Response Time

6.2.1. Normally Black Type (Negative)

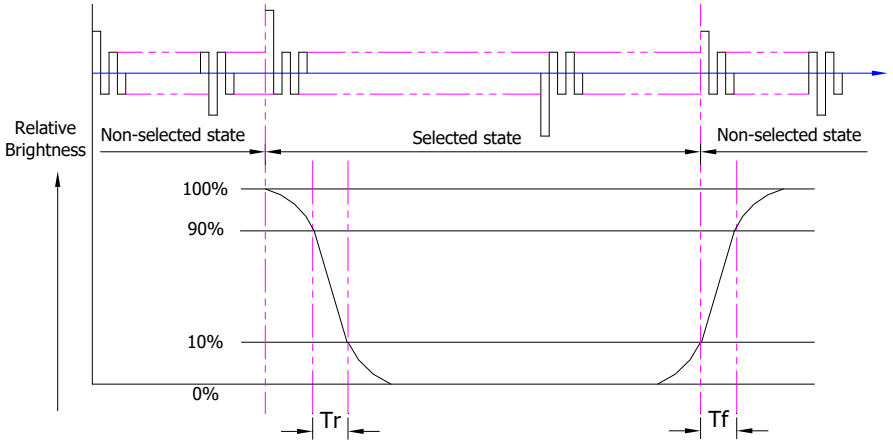


Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note : Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note : Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

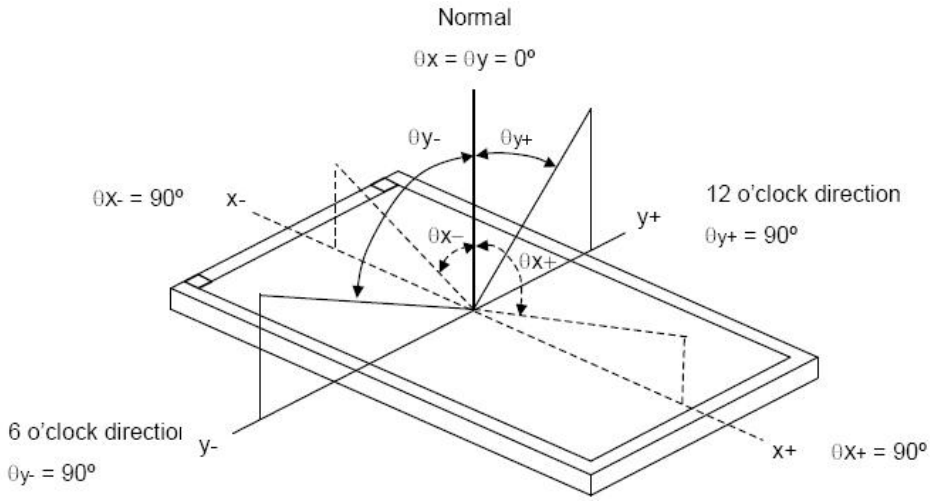
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



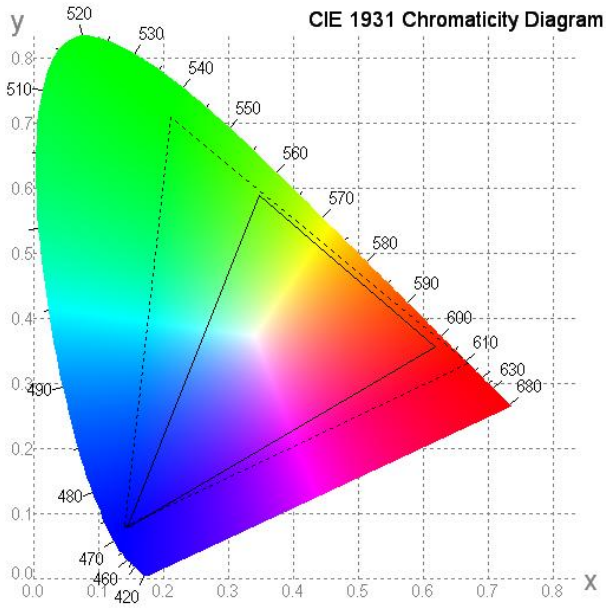
Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

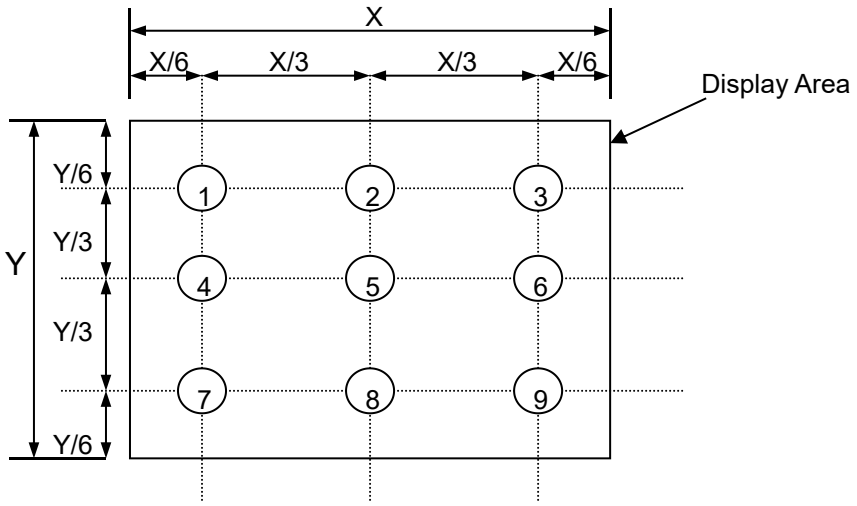
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

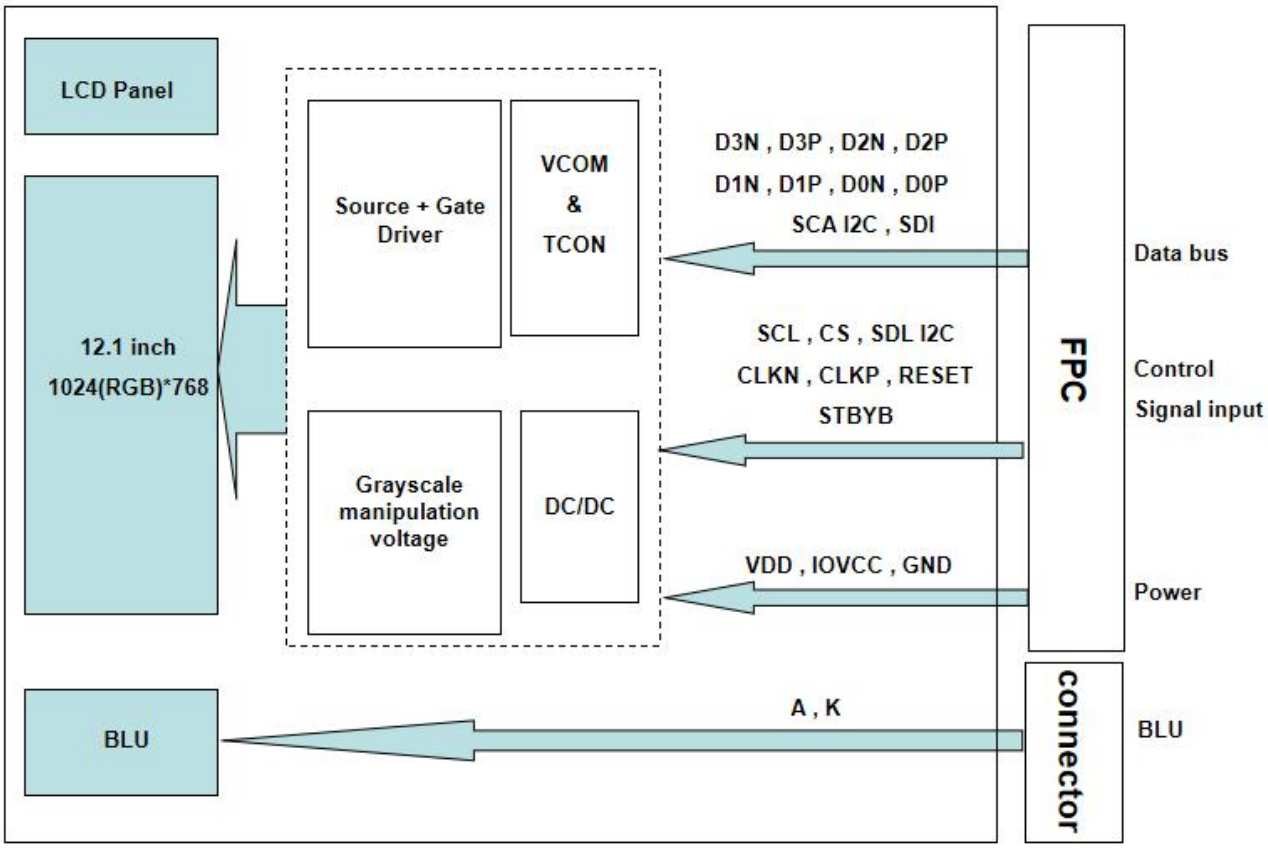
6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7



7. Block Diagram and Power Supply



8. Interface Pins Definition

No.	Symbol	Function	Remark
1	VGLO	Output voltage from the step-up circuit. Connect to a stabilizing capacitor between VGL and system ground. Place a Scotty barrier diode between AVEE and VGL. Place a Scotty barrier diode between VGL and system ground. (Optional)	
2	VGHO	Output voltage from the step-up circuit. Connect to a stabilizing capacitor between VGH and system ground. Place a Scotty barrier diode between AVDD and VGH. (Optional) The diode is needed when AVDD come from external power	
3	VSN	Input negative power from system/ external power IC	
4	VSN	Input negative power from system/ external power IC	
5	VSP	Input positive power from system/ external power IC	
6	VSP	Input positive power from system/ external power IC	
7	NC	No connection	
8	SCL	Serial clock input in SPI interface (CMDSEL=1) If not use, let it open or IOVCC or GND	
9	SDI	Serial data input / output pin in SPI interface operation (CMDSEL=1). If not use, let it open	
10	CS	Chip select pin. (CMDSEL=1) 0: Chip can be accessed; 1: Chip cannot be accessed. If this pin is not used, please connect it to IOVCC	
11	VDD	Power supply	
12	BIST	No connection	
13	SCA I2C	Serial data input / output pin in I2C interface operation. (CMDSEL=0). If use I2C interface, reserve 4.7Kohm resistance to IOVCC on FPC. If not use, please connect it to IOVCC.	
14	SDL I2C	Serial clock input in I2C interface. (CMDSEL=0) If use I2C interface, reserve 4.7Kohm resistance to IOVCC on FPC. If not use, please connect it to IOVCC	
15	NC	No connection	
16	IOVCC	I/O Power supply	
17	IOVCC	I/O Power supply	
18	IOVCC	I/O Power supply	
19	GND	Ground	
20	D3P	LVDS/MIPI-DSI Data differential signal input pins. (Data lane 3) if not used , Please connected to VSSH or open	
21	D3N	LVDS/MIPI-DSI Data differential signal input pins. (Data lane 3) if not used , Please connected to VSSH or open	
22	GND	Ground	

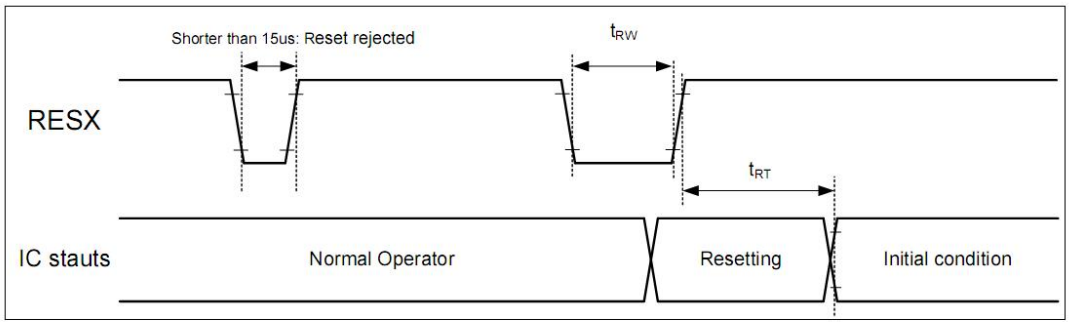
<table>
<tr><td>23</td><td>CLKP</td><td>LVDS/MIPI-DSI CLOCK differential signal input pins.
if not used , Please connected to VSSH or open</td><td></td></tr>
<tr><td>24</td><td>CLKN</td><td>LVDS/MIPI-DSI CLOCK differential signal input pins.
if not used , Please connected to VSSH or open</td><td></td></tr>
<tr><td>25</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>26</td><td>D2P</td><td>LVDS/MIPI-DSI Data differential signal input pins. (Data lane 2)
if not used , Please connected to VSSH or open</td><td></td></tr>
<tr><td>27</td><td>D2N</td><td>LVDS/MIPI-DSI Data differential signal input pins. (Data lane 2)
if not used , Please connected to VSSH or open</td><td></td></tr>
<tr><td>28</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>29</td><td>D1P</td><td>LVDS/MIPI-DSI Data differential signal input pins. (Data lane 1)
if not used , Please connected to VSSH or open</td><td></td></tr>
<tr><td>30</td><td>D1N</td><td>LVDS/MIPI-DSI Data differential signal input pins. (Data lane 1)
if not used , Please connected to VSSH or open</td><td></td></tr>
<tr><td>31</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>32</td><td>D0P</td><td>LVDS/MIPI-DSI Data differential signal input pins. (Data lane 0)
if not used , Please connected to VSSH or .open</td><td></td></tr>
<tr><td>33</td><td>D0N</td><td>LVDS/MIPI-DSI Data differential signal input pins. (Data lane 0)
if not used , Please connected to VSSH or .open</td><td></td></tr>
<tr><td>34</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>35</td><td>RESET</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset (active low) after power is supplied</td><td></td></tr>
<tr><td>36</td><td>STBYB</td><td>Standby mode<table><tr><td>STBYB</td><td>IC Status</td></tr><tr><td>0</td><td>Standby Mode</td></tr><tr><td>1</td><td>Normal Mode</td></tr></table></td><td></td></tr>
<tr><td>37</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>38</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>39</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>40</td><td>NC</td><td>No connection</td><td></td></tr>
</table>

BLU:

No.	Symbol	Function
1	A	Backlight anode
2	K	Backlight cathode

9. AC Characteristics

9.1. Reset Timing



Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset "L" pulse width(2)	RESX	20	-	µs
t_{RT}	Reset complete time(3)	-	-	5(5)	ms
		-	-	120(6) (7) (8)	ms

Note:

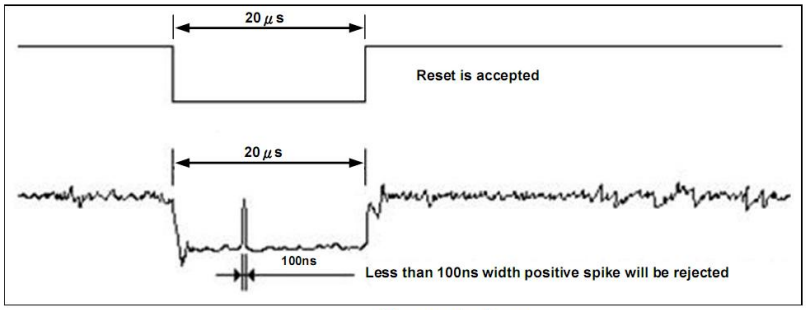
(1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 µs	Reset Rejected
Longer than 20 µs	Reset
Between 15 µs and 20 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

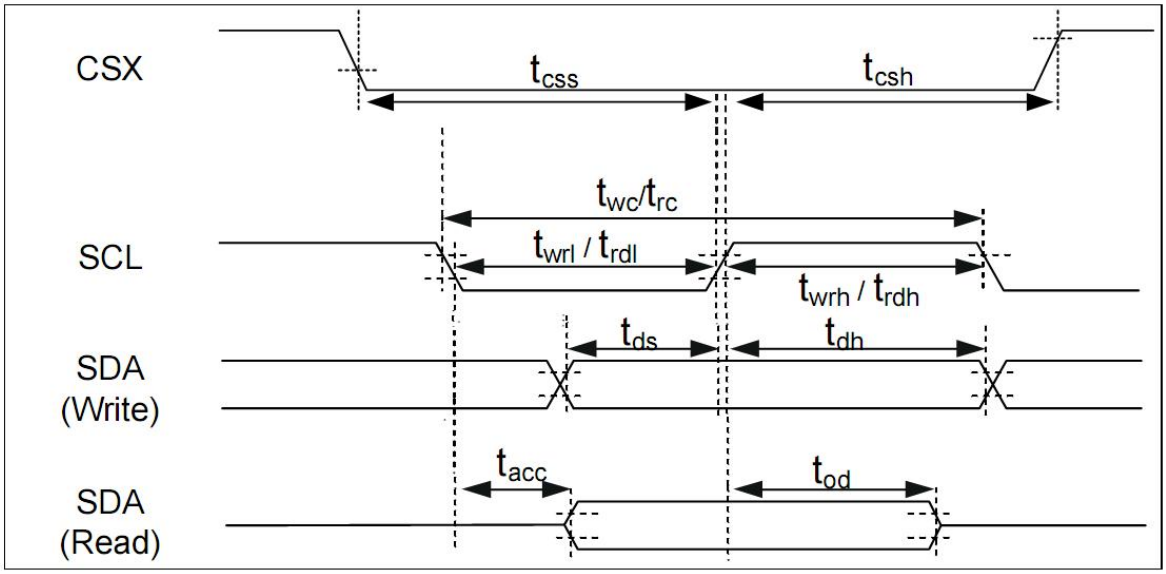


Reset timings

(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

9.2. SPI electronic characteristics



: SPI interface AC characteristics

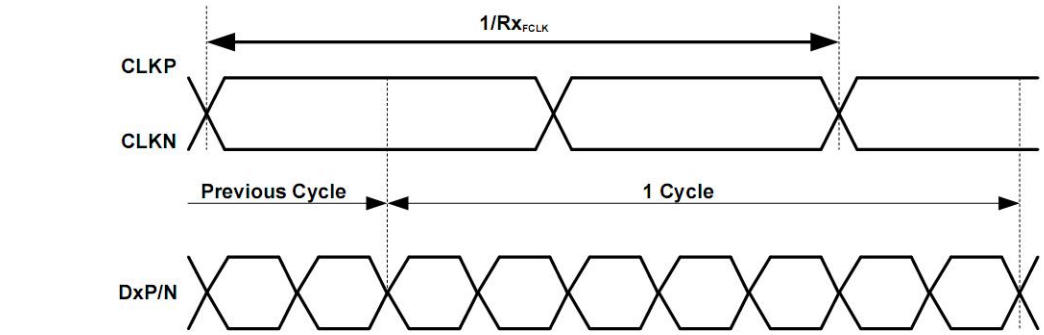
(T_A=25°C, IOVCC=3.3V, VCI=3.3V)

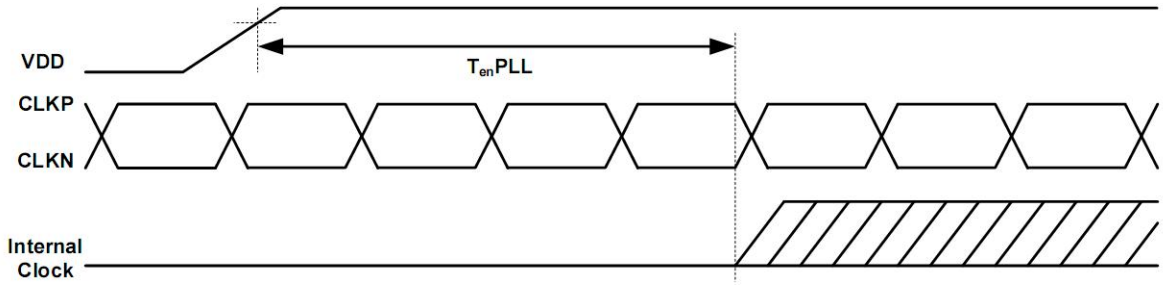
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css} t_{csh}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
SCL (Write)	t_{wc} t_{wrh} t_{wrl}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 40 40	- - -	ns	-
SCL (Read)	t_{rc} t_{rdh} t_{rdl}	Read cycle Control pulse “H” duration Control pulse “L” duration	150 60 60	- - -	ns	-
SDA (Write)	t_{ds} t_{dt}	Data setup time Data hold time	30 30	- -	ns	Note(1)
SDA (Read)	t_{acc} t_{od}	Read access time Output disable time	- 10	35 50	ns	

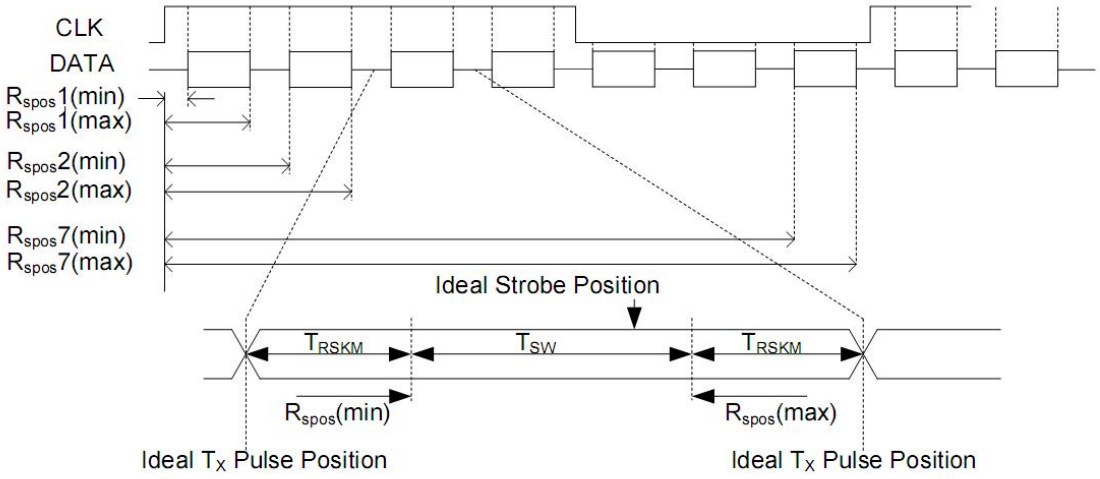
Note: (1) For maximum C_L=30pF, for minimum C_L=8pF.
(2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(3) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

: SPI interface AC characteristics

9.3. LVDS electronic characteristics







T_{SW}: Strobe width (Internal data sampling window)
R_{spos} : Receiver strobe position
T_{RSKM} : Receiver strobe margin

: LVDS AC characteristics

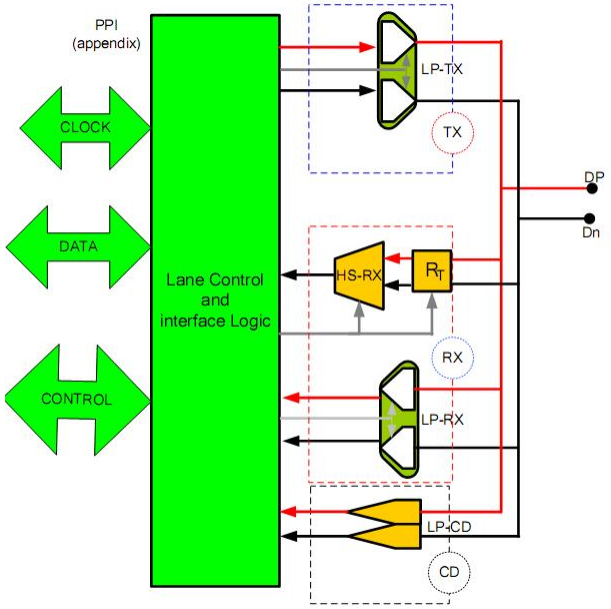
Signal	Symbol	Min.	Typ	Max.	Unit	Description
Clock frequency	Rx_{FCLK}	30	-	75	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V @Rx_{FCLK}=75MHz
Clock high time	T_{LVCH}	-	4/(7x Rx_{FCLK})	-	ns	-
Clock low time	T_{LVCL}	-	3/(7xRx_{FCLK})	-	ns	-
PLL wake-up time	T_{en}PLL	-	-	150	us	-

: LVDS AC characteristics

9.4. DSI D-PHY electronic characteristics

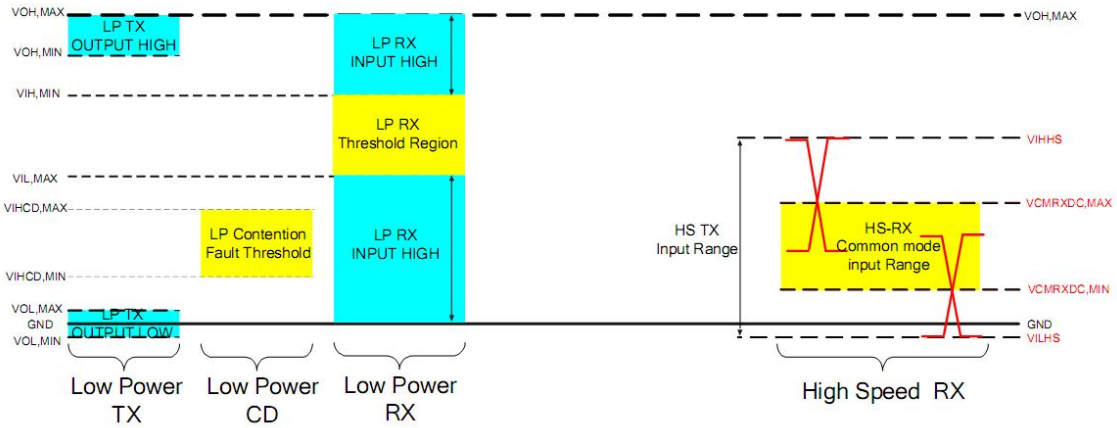
The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 11.5 shows the complete set of electronic functions required for a fully featured PHY transceiver.



Electronic functions of a D-PHY transceiver

Figure shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.



HS and LP signal levels

The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30-0.075 * (VO, INST-700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

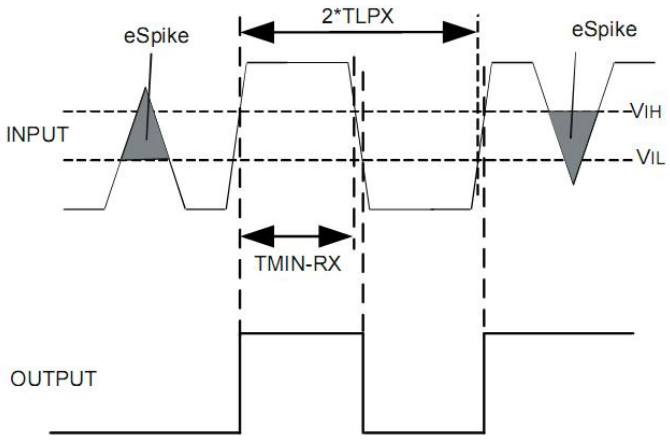
LP-TX AC Specifications

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 11.7 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.



Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

LP-RX AC Specifications

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.

2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Contention Detector DC Specifications

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

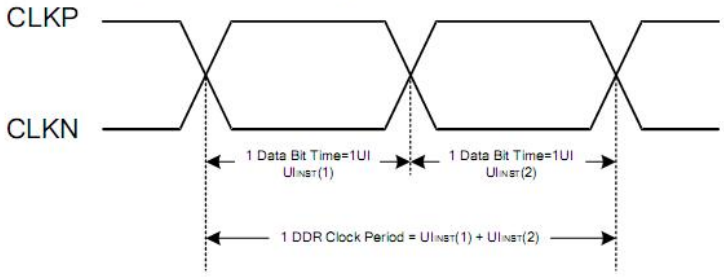
Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

HS Receiver AC Specifications

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure



DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	3.33	ns	(1), (2), (3), (4), (5)

Note: (1) This value corresponds to a minimum 300 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 630Mbps/per lane of 2 data lanes 24-bit data format
(4) Maximum total bit rate is 600Mbps/per lane of 3 data lanes 24-bit data format
(5) Maximum total bit rate is 500Mbps/per lane of 4 data lanes 24-bit data format

Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 11.9. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

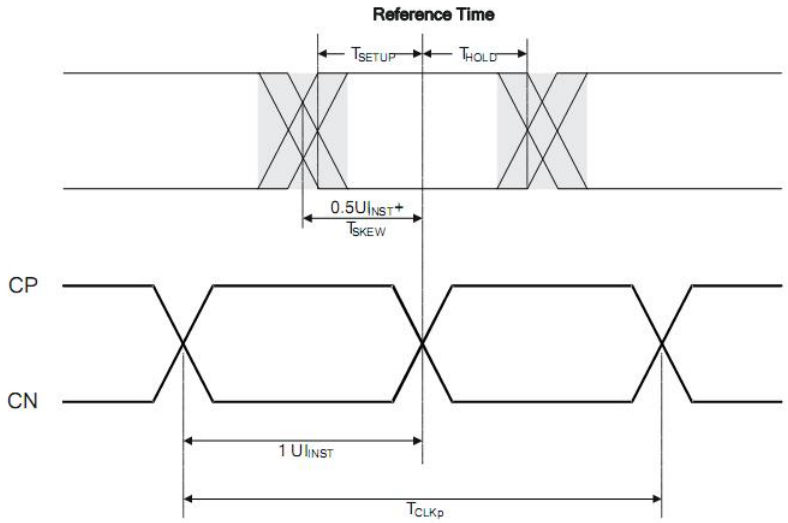


Figure 11.9: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 11.15. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 11.15 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

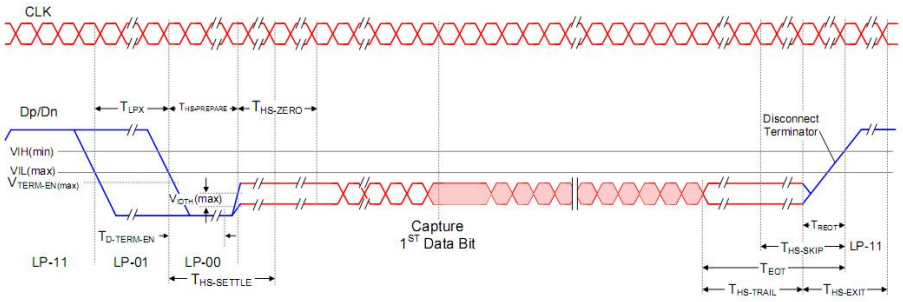
The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

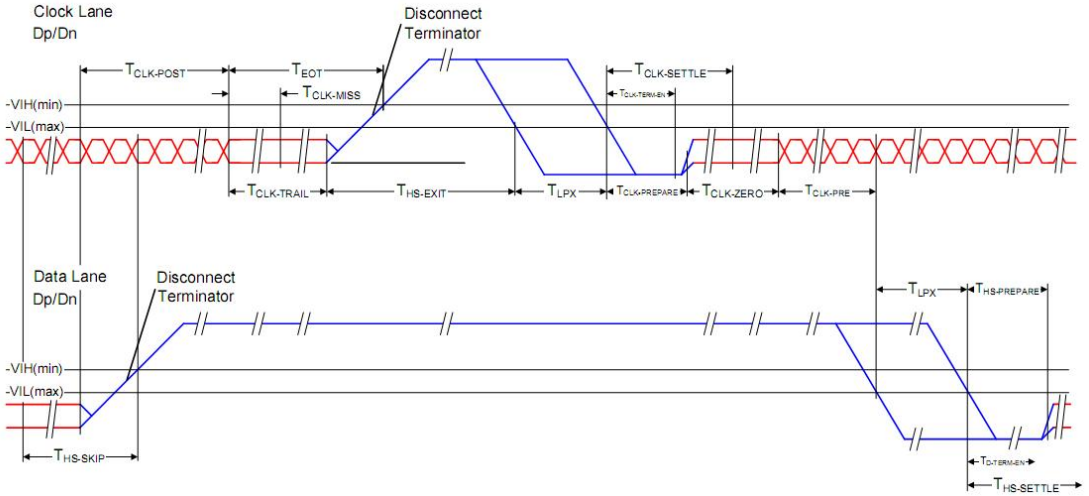
Data to Clock Timing Specifications

Burst Mode Data Transmission



High-Speed Data Transmission in Bursts

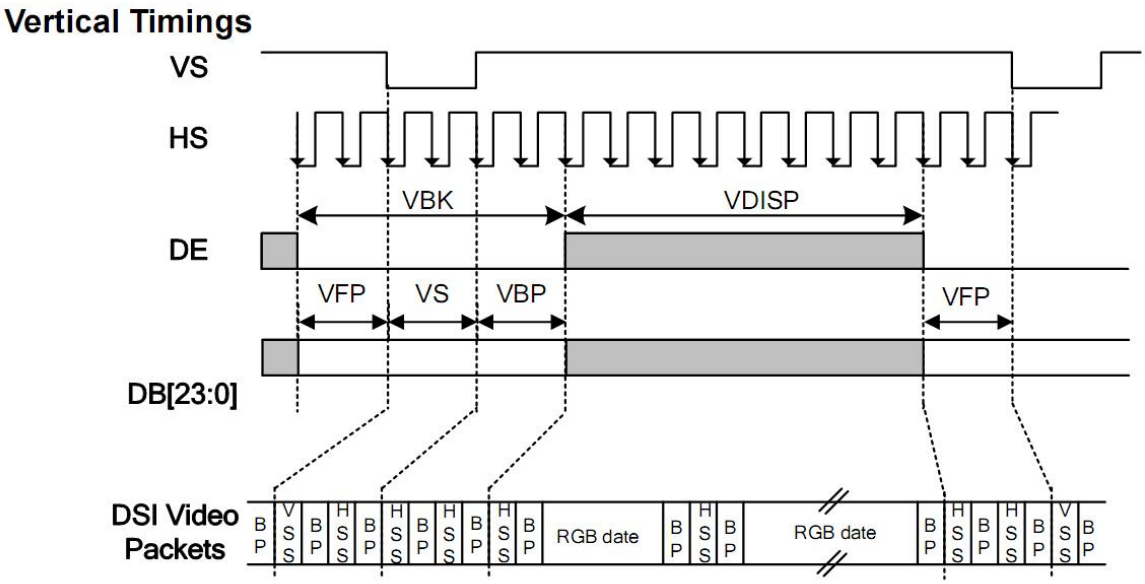
Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60+n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns



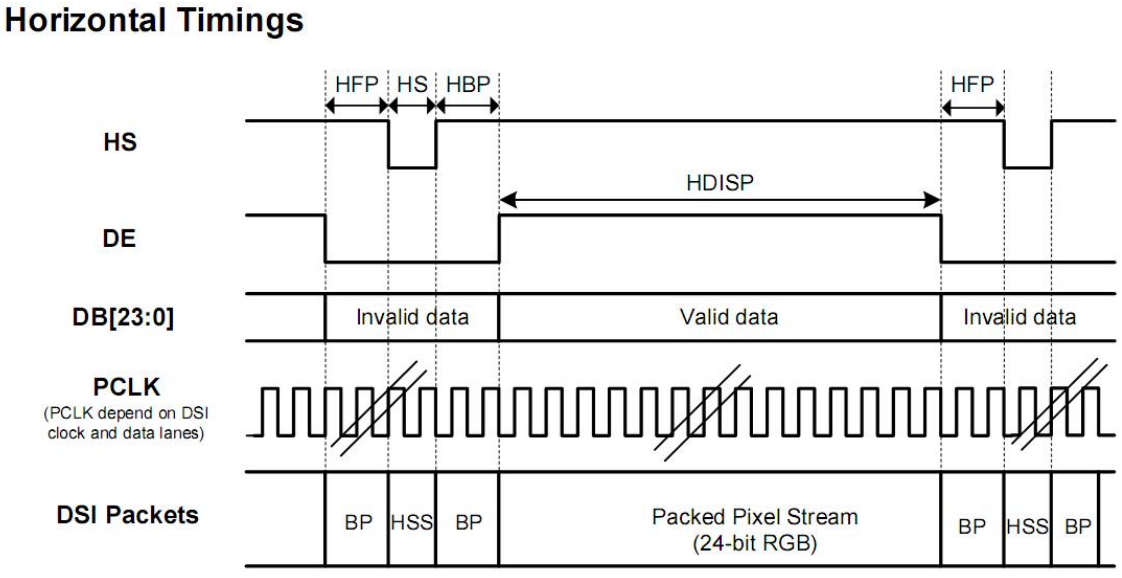
: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

9.5. Timing for DSI Video mode



: Vertical Timings for DPI I/F



: Horizontal Timing for DSI Video mode I/F

9.6. RGB timing table

TBD

10. Quality Assurance

10.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

10.2. Standard for Quality Test

10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

10.3. Nonconforming Analysis & Disposition

10.3.1. Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

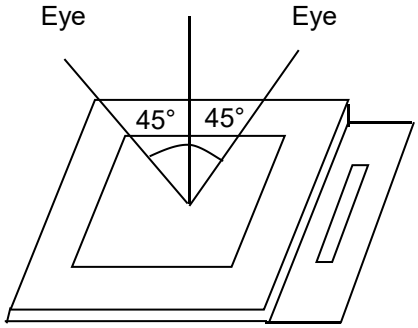
10.5. Standard of the Product Visual Inspection

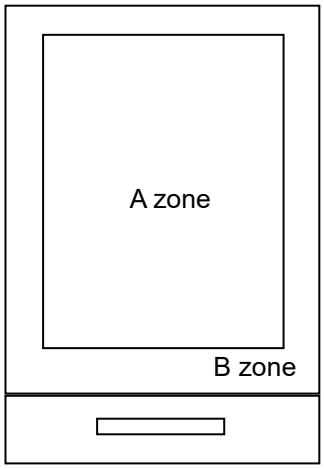
10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



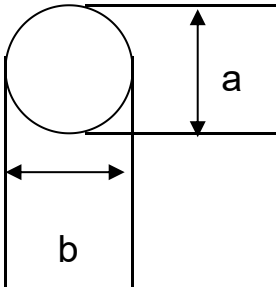


10.5.2. Basic principle:

10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

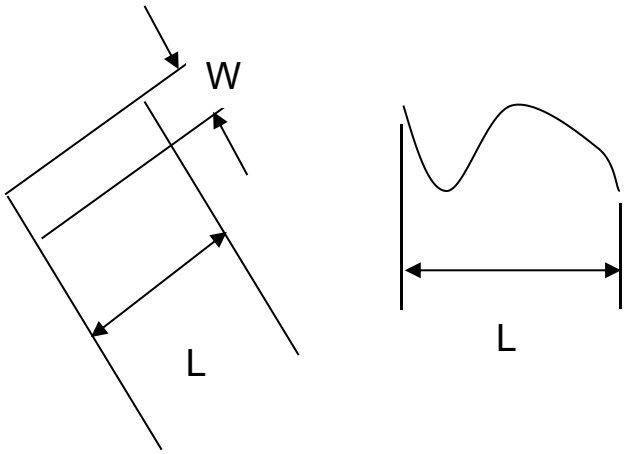
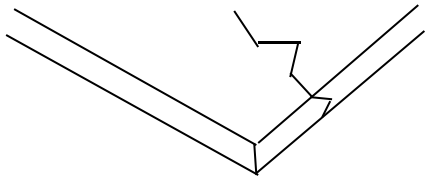
10.5.2.2. New item must be added on time when it is necessary.

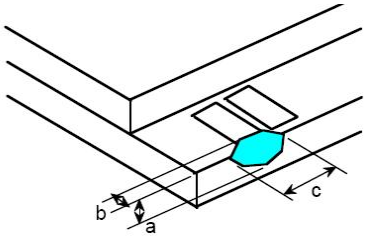
10.6.Inspection Specification

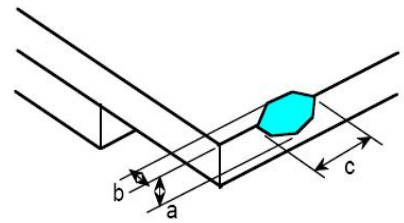
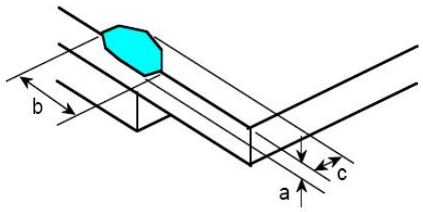
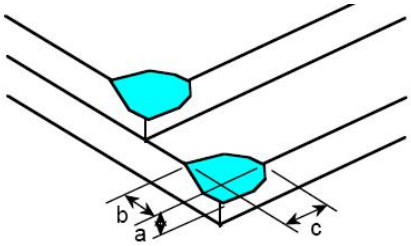
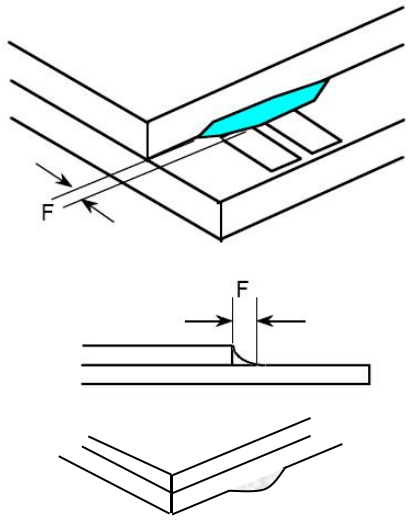
<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material
(Round type)
Pinholes
Stain
Particles inside cell.
(Minor defect)</td><td>


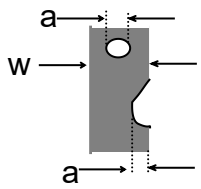
φ= (a + b) /2

<table>
<tr><th>Size \ Area</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.20</td><td>Ignore</td></tr>
<tr><td>0.20<φ≤0.50</td><td>N≤3</td></tr>
<tr><td>0.50<φ</td><td>0</td></tr>
</table>
Distance between 2 defects should more than 5mm apart.
</td></tr>
<tr><td>02</td><td>Electrical Defect
(Minor defect)</td><td>
<table>
<tr><td rowspan="2">Bright dot</td><td>Display Area</td><td>Total</td><td rowspan="4">Note1</td></tr>
<tr><td>N≤2</td><td>N≤2</td></tr>
<tr><td>Dark dot</td><td>N≤4</td><td>N≤4</td></tr>
<tr><td>Total dot</td><td>N≤4</td><td>N≤4</td></tr>
<tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note 2</td></tr>
</table>
Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.
</td></tr>
</table>

03	Black and White line Scratch Foreign material (Line type) (Minor defect)	 Length / Width / Acc. Qty / / W ≦ 0.1 / Ignore L ≦ 2.5 / 0.1 ＜ W ≦ 0.2 / 3 L＞2.5 / 0.2 ＜ W / 0 Total / 3 Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
04	Glass Crack (Minor defect)	 Crack is potential to enlarge, any type is not allowed.

05	Glass Chipping Pad Area: (Minor defect) 	Length and Width / Acc. Qty c > 3.0, b< 1.0 / 1 c< 3.0, b< 1.0 / 3 a<Glass Thickness

<table>
<tr>
<td>06</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>07</td>
<td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>08</td>
<td>Glass Corner Chipping:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>09</td>
<td>Glass Burr:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length</th><th>Acc. Qty</th></tr>
<tr><td>F < 1.0</td><td>Ignore</td></tr>
</table>
Glass burr don’t affect assemble and module dimension.</td>
</tr>
</table>

<table>
<tr><td>10</td><td>FPC Defect:
(Minor defect)
 
</td><td>10.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
10.2 Open circuit is unacceptable.
10.3 No oxidation, contamination and distortion.</td></tr>
<tr><td>11</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.30</td><td>Ignore</td></tr><tr><td>0.30 <φ≤0.50</td><td>N≤2</td></tr><tr><td>0.50 < φ</td><td>N=0</td></tr></table></td></tr>
<tr><td>12</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.25</td><td>Ignore</td></tr><tr><td>0.25 <φ≤0.50</td><td>N≤4</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>13</td><td>Bezel</td><td>13.1 No rust, distortion on the Bezel.
13.2 No visible fingerprints, stains or other contamination.</td></tr>
<tr><td>14</td><td>PCB</td><td>14.1 No distortion or contamination on PCB terminals.
14.2 All components on PCB must same as documented on the BOM/component layout.
14.3 Follow IPC-A-600F.</td></tr>
<tr><td>15</td><td>Soldering</td><td>Follow IPC-A-610C standard</td></tr>
<tr><td>16</td><td>Electrical Defect
(Major defect)</td><td>The below defects must be rejected.
16.1 Missing vertical / horizontal segment,
16.2 Abnormal Display.
16.3 No function or no display.
16.4 Current exceeds product specifications.
16.5 LCD viewing angle defect.
16.6 No Backlight.
16.7 Dark Backlight.
16.8 Touch Panel no function.</td></tr>
</table>

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7. Classification of Defects

10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

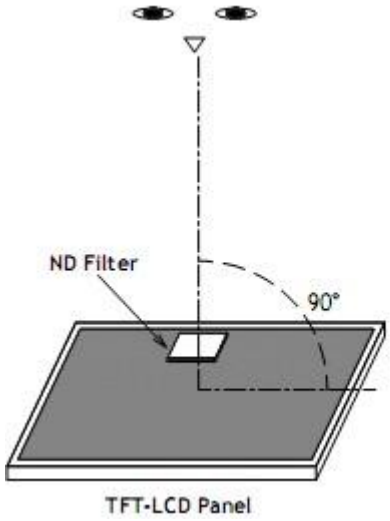
10.9. Packaging

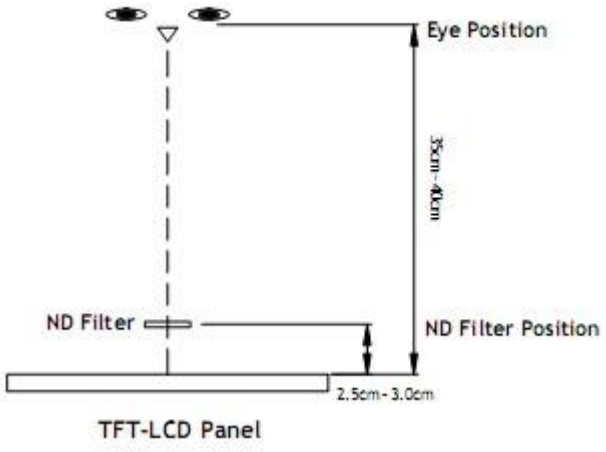
10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

10.9.2. Modules inside package box should have compliant mark.

10.9.3. All direct package materials shall offer ESD protection

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.





Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

11. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	**50℃, 96Hrs**	2	GB/T2423.2 -2008
2	Low Temperature Operating	**-0℃, 96Hrs**	2	GB/T2423.1 -2008
3	High Humidity Storage	**50℃, 90%RH, 96Hrs**	2	GB/T2423.3 -2016
4	High Temperature Storage	**60℃, 96Hrs**	2	GB/T2423.2 -2008
5	Low Temperature Storage	**-10℃, 96Hrs**	2	GB/T2423.1 -2008
6	Thermal Cycling Test Storage	-30℃, 60min~80℃, 60min, 20 cycles.	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X,Y,Z 30 min for each direction.	-	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times	2	GB/T17626.2 -2018
		Contact:±2KV 150pF/330Ω 5 times		
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.7 -2018

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

12. Precautions and Warranty

12.1.Safety

12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2.Handling

12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3.Storage

12.3.1. Do not store the LCD module beyond the specified temperature ranges.

12.3.2. Strong light exposure causes degradation of polarizer and color filter.

12.4.Metal Pin (Apply to Products with Metal Pins)

12.4.1. Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

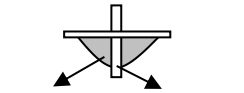
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

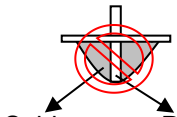
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting



Recommended



Not Recommended

12.4.2. Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

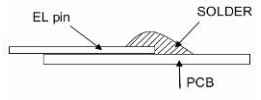
Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

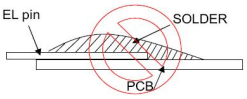
12.4.2.4. No horizontal press on the EL leads during soldering.

12.4.2.5. 180° bend EL leads three times is not allowed.

12.4.2.6. Solder Wetting

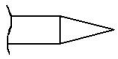


Recommended

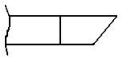


Not Recommended

12.4.2.7. The type of the solder iron:

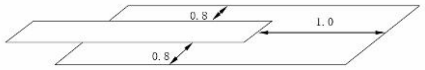


Recommended



Not Recommended

12.4.2.8. Solder Pad



12.5. Operation

12.5.1. Do not drive LCD with DC voltage

12.5.2. Response time will increase below lower temperature

12.5.3. Display may change color with different temperature

12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

12.5.5. Do not connect or disconnect the LCM to or from the system when power is on.

12.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.

12.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

12.5.8. Do not display the fixed pattern for long time（we suggest the time not longer than one hour）because it will develop image sticking due to the TFT structure.

12.6. Static Electricity

12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

12.6.2. The normal static prevention measures should be observed for work clothes and benches.

12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

12.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

12.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

12.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

13. Packaging

TBD

14. Outline Drawing