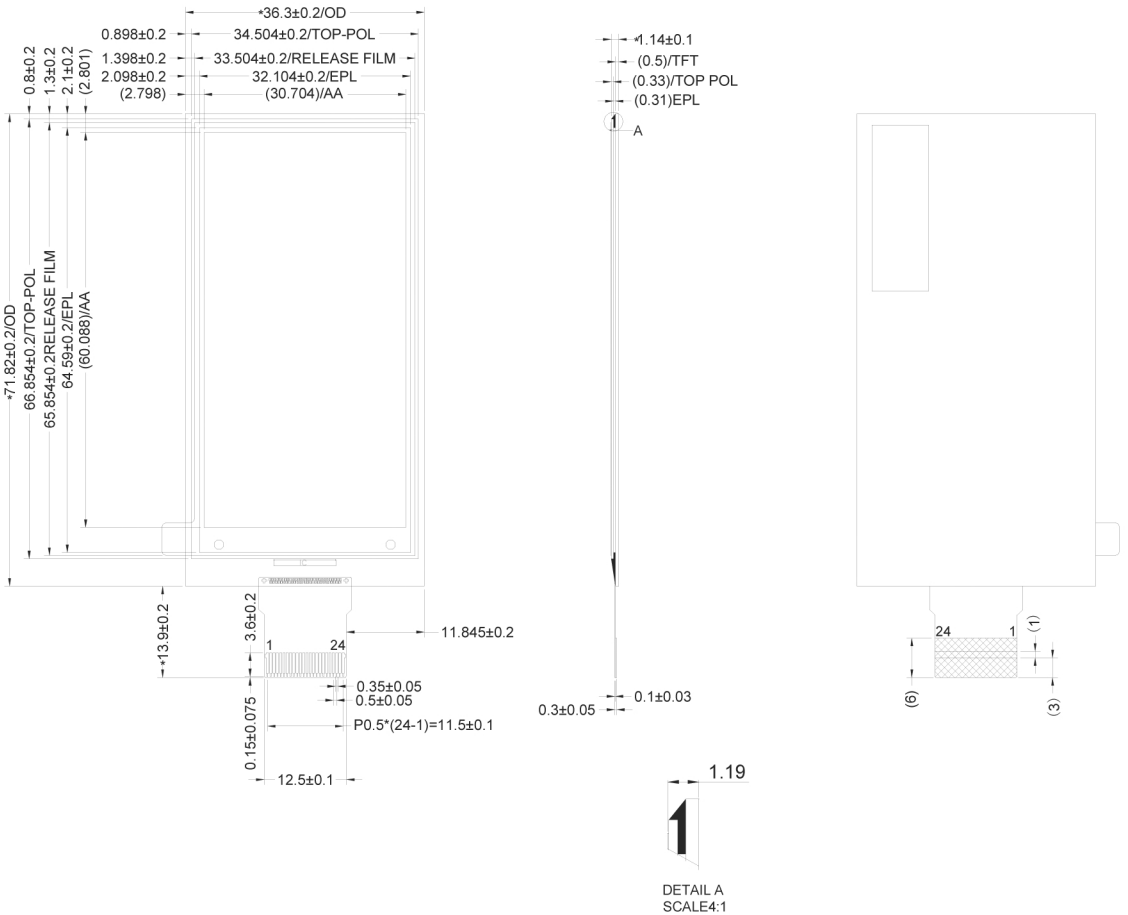

PIN	PIN NAME
1	NC
2	GDR
3	RESE
4	NC
5	VDHR
6	TSCL
7	TSDA
8	BS
9	BUSYN
10	RSTN
11	D/C
12	CSB
13	SCL
14	SDA
15	VDD
16	VDD
17	VSS
18	VDDD
19	VPP
20	VSH
21	VGH
22	VSL
23	VGL
24	VCOM

Compliance: RohS III (2015/863/EU)

NOTES：
1.Dispaly mode 2.6" arrey for EPD;
2.Unspecified Tolerance:±0.20;
3.Material conform to the RoHS standard;
4.Mark" * "for control DIM.reference dimension in ( )

Tolerances:			Date	Name
			06/24	dr
Modifications	Date	Name		

YDP EI 260 M

knitter-switch

30 54 38

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PRODUCT SPECIFICATION

2.6” EPD MODULE

MODEL: YDP EI 260 M **Ver:1.0**

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
TFT S. G. H 20220929			TFT L. Q 20220929

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2022.09.29	LQ	Initial Release	

Table of Contents

1. General Description

The Product is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 2.6” active area contains 152x296 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	2.6”	
Resolution	152(H) X 296 (V)	Pixels
Module Outline	36.3(H) x 71.82(V) x 1.14(T) (Note1)	mm
Active Area	30.704 (H) x 60.088(V)	mm
Pixel Pitch	202(H) x 203(V)	um
Pixel configuration	Rectangle	
Operating Temperature	**0～50**	ºC
Storage Temperature	**-25～70**	ºC
Weight	(7)	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Electrical Characteristics

3.1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{dd} +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{dd} +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

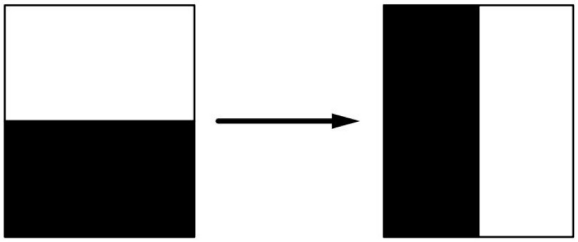
3.2. Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{dd}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{dd}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{dd}	V
OTP Program voltage	V_{PP}	-	VPP	-	8.25	-	V
Typical power panel	P_{TYP}	-	-	-	12	120	mW
Deep sleep mode	P_{STPY}	-	-	-	4.0	-	uW
Typical operating current	Iopr_VDD	V_{dd} =3.0V-	-	-	4.0	10	mA
Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	26	--	uA
Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	1	--	uA
Operation temperature range	T_{OPR}	-	-	0	-	35	°C
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux
Storage temperature range	T_{STG}	-	-	-25	-	60	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes:

1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.



The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.

3.3. Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM		-1.6		V

4. Optical Characteristics

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		8:1	10:1	-	-	11-2
White△L 24h	Reduce		-	≤4	-	-	-
T_{update}	Image update time	at 25 °C	-	2800	-	ms	-

Notes:

1. Luminance meter: Eye-One Pro Spectrophotometer.
2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

5. Interface Pins Definition

No.	Symbol	Function	Remark
1	NC	Do not connect with other NC pins	
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	Do not connect with other NC pins	
5	VDHR	Positive Source driving voltage 1	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Data pin	
8	BS	Bus Interface selection pin	Note 4
9	BUSYN	Busy state output pin	Note 3
10	RSTN	Reset signal input. Active Low.	
11	D/C	Data /Command control pin	Note 2
12	CSB	Chip select input pin	Note 1
13	SCL	Serial Clock pin (SPI)	
14	SDA	Serial Data pin (SPI)	
15	VDD	Power Supply for interface logic pins	
16	VDD	Power Supply for the chip	
17	VSS	Ground	
18	VDDD	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	Power Supply for OTP Programming	
20	VSH	Positive Source driving voltage 2	
21	VGH	Positive Gate driving voltage	
22	VSL	Negative Source driving voltage	
23	VGL	Negative Gate driving voltage	
24	VCOM	VCOM driving voltage	

Note1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin Low when

- Outputting display waveform

- Programming with OTP

- Communicating with digital temperature sensor

Note 4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. AC Characteristics

6.1. MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Connnand Interface		Control Signal		
Bus interface	SDA	SCL	CSB	D/C	RSTN
4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
3-wire SPI	SDIN	SCLK	CSB	L	RSTN

MCU interface assignment under different bus interface mode

6.2. MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

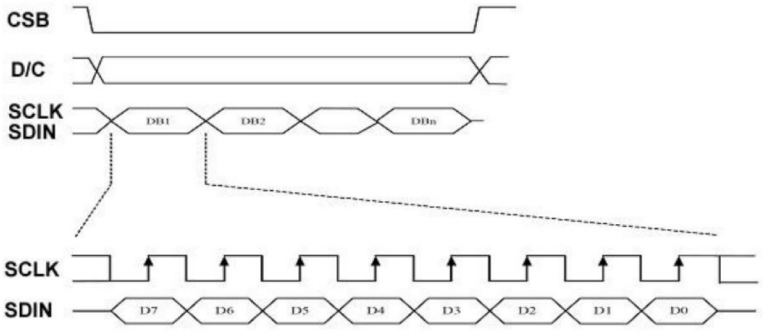
Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.



Write procedure in 4-wire SPI mode

6.3. MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

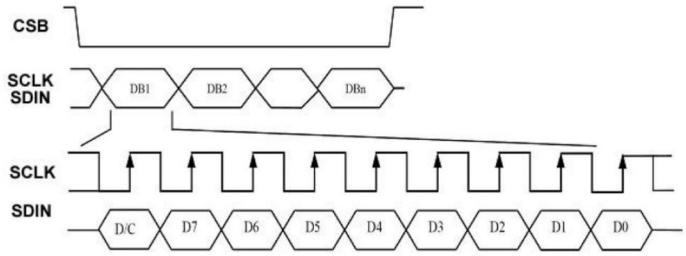
The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

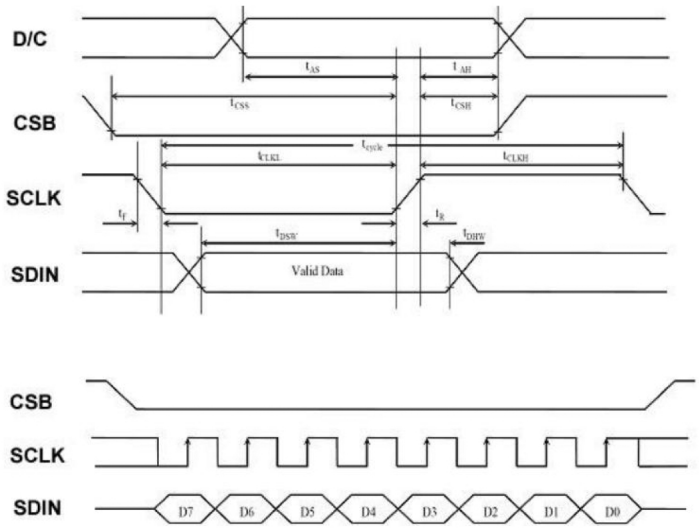
Control pins of 3-wire Serial interface



Write procedure in 3-wire SPI mode

6.4. Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, TOPR =25ºC.



Serial interface characteristics

(V_{dd} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~80%]	-	-	15	ns

Serial Interface Timing Characteristics

7. Handling, Safety, and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it.
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel.
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet.
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature,high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15ºC to 35ºC, and humidity from 30%RH to 60%RH.

8. Reliability Specification

No	Item	Condition	Quantity	Method
1	High Temperature Operating	**+50°C, RH = 30% ,240Hrs**	2	IEC 60 068-2-2Bp
2	Low Temperature Operating	**0℃, 240Hrs**	2	IEC 60 068-2-2Ab
3	High Humidity Storage	**60℃, 80%RH, 240Hrs**	2	IEC 60 068-2-3CA
4	High Temperature Storage	**+70℃,RH = 23% ,240Hrs**	2	IEC 60 068-2-2Bp
5	Low Temperature Storage	**-25℃, 240Hrs**	2	IEC 60 068-2-1Ab
6	Thermal Cycling Test Storage	-25℃, 30min~70℃, 30min, 100 cycles.	2	IEC 60 068-2-14
7	Packing vibration	Frequency range:10~500Hz Acceleration of gravity:1.04G X,Y,Z 60 min for each direction.	-	Full packed for shipment
8	Electrical Static Discharge	Machine model +/- 250V, 0Ω , 200pF	2	IEC 62179, IEC 62180
9	Drop Test (Packaged)	Height:122 cm,1 corner, 3 edges, 6 surfaces.	-	Full packed for shipment

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

9. Packaging

TBD